Seat No.: _____   Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER–IV (NEW) EXAMINATION – WINTER 2021

Subject Code:2140707   **Date:24/12/2021**
Subject Name:Computer Organization
Time:10:30 AM TO 01:00 PM   **Total Marks: 70**
Instructions:
  1. **Attempt all questions.**
  2. **Make suitable assumptions wherever necessary.**
  3. **Figures to the right indicate full marks.**
  4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Define: microinstruction; Draw different types of 16 bits instruction formats.	**03**
	(b)	Describe Construction of a Common bus system for three state buffers with diagram.	**04**
	(c)	What is binary adder? Construct diagram of 4-bits binary adder and explain it.	**07**
Q.2	**(a)**	Explain BSA and ISZ instruction as a memory reference instruction.	**03**
	(b)	What is memory read and memory write operation? Explain with the help of DR (data register) and AR (address register) using diagram.	**04**
	(c)	What is the role of sequence counter (SC) in control unit? Explain with the help of its three inputs.	**07**
		OR	
	(c)	Construct and explain 4-bit combinational circuit shifter diagram.	**07**
Q.3	**(a)**	List out any five memory reference instructions with their short symbolic description.	**03**
	(b)	List out names of eight main registers of basic computer with their symbolic name and purpose.	**04**
	(c)	Describe Register transfer for fetch and decode phase in Instruction pipeline with its diagram.	**07**
		OR	

Q.3	**(a)**	Explain following terms.
		  I. Mapping of Instruction.
		  II. Subroutine.
			03

	(b)	Differentiate RISC and CISC.	**04**
	(c)	Explain Three-Address Instructions, One Address instructions and zero address instruction with common example.	**07**
Q.4	**(a)**	Write and explain symbolic forms of CD and BR fields of microinstructions.	**03**
	(b)	Explain memory hierarchy in a computer system.	**04**
	(c)	What is interrupt? Explain different types of interrupt.	**07**
		OR	
Q.4	**(a)**	Discuss 20 bit Microinstruction code format in short.	**03**
	(b)	What is cache memory? Discuss direct address mapping with diagram.	**04**
	(c)	Define: Addressing Mode; Describe relative addressing mode and immediate addressing mode with diagram.	**07**

Q.5	**(a)**	Explain Asynchronous Data Transfer with Handshaking example.	**03**
	(b)	Explain flynn's classification with proper diagram.	**04**
	(c)	List out modes of transfer. Discuss direct memory access (DMA) technique.	**07**

OR

Q.5	**(a)**	Explain four-segment instruction pipeline.	**03**
	(b)	Explain major hazards in pipelined execution.	**04**
	(c)	Draw and explain flowchart of CPU-IOP communication.	**07**

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